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1 **ABSTRACT OF THE DISCLOSURE**

2 An SRAM memory cell having first and second transfer
3 gate transistors. The first transfer gate transistor
4 includes a first source/drain connected to a bit line and
5 the second transfer gate transistor has a first
6 source/drain connected to a complement bit line. Each
7 transfer gate transistor has a gate connected to a word
8 line. The SRAM memory cell also includes first and second
9 pull-down transistors configured as a storage latch. The
10 first pull-down transistor has a first source/drain
11 connected to a second source/drain of said first transfer
12 gate transistor; the second pull-down transistor has a
13 first source/drain connected to a second source/drain of
14 said second transfer gate transistor. Both first and
15 second pull-down transistors have a second source/drain
16 connected to a power supply voltage node. The first and
17 second transfer gate transistors each include a gate oxide
18 layer having a first thickness, and the first and second
19 pull-down transistors each include a gate oxide layer
20 having a second thickness, wherein and the first thickness
21 is different from the second thickness.